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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,275	06/10/2005	Elstan Anthony Fernandez	1890-0257	9417

7590 08/08/2006

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EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/538,275	FERNANDEZ ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-35* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9-28-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Examiner acknowledges claims 1-15 have been cancelled. Newly admitted claims 16-35 have been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 27 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Seyyedy (6,780,675 B2).

2. Regarding claim 27, Seyyedy discloses a substrate, comprising: a plurality of first contacts (Figure 3, reference 104) and a first face (Figure 3, reference 106) configured to attach to a first integrated circuit (Figure 3, reference 102) with electrical connection between the first contacts and the first integrated circuit (Figure 1); a plurality of second contacts (Figure 3, reference 204) and a second face (Figure 3, reference 206) configured to attach to a second integrated circuit (Figure 3, reference 202) with electrical connection between the second contacts and the second integrated circuit (Figure 2); wherein the substrate defines a plurality of holes extending between the first face and the second face (Figure 2, reference 218), the substrate is laminar (Figure 2, reference 216) and at least the first face includes solder balls (column 1, lines 23-46).

3. Regarding claim 28, Seyyedy discloses wherein the solder balls are arranged in an array having a region without solder balls, and wherein said region is configured to receive the first integrated circuit (column 1, lines 23-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seyyedy (6,780,675 B2) in view of Chhor et al (6,843,421 B2).

4. Regarding claim 16, Seyyedy discloses a method of packaging integrated circuits comprising: attaching a first integrated circuit (Figure 3, reference 102) to a first face of a substrate (Figure 3, reference 216) with electrical connection between corresponding contacts of the substrate and the first integrated circuit (Figure 3, reference 104); attaching a second integrated circuit (Figure 3, reference 202) to a second face of the substrate with electrical connection between electrical contacts of the substrate and the second integrated circuit (Figure 3, reference 204). However, Seyyedy does not disclose encasing the first and second integrated circuits in resin.

Chhor et al discloses encasing the first and second integrated circuits in resin (abstract).

It is obvious, at the time the invention was made, for one having ordinaryskill in the art, to modify Seyyedy with the teachings of Chhor et al, for the purpose of creating a memory module.

Claims 17-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seyyedy (6,780,675 B2) and Chhor et al (6,843,421 B2) in view of Thummel (US 2001/0045686 A1).

5. Seyyedy and Chhor et al discloses all above claimed subject matter except wherein the substrate includes holes extending between the first face and the second face, the encasing step includes applying the resin to a first side of the substrate and flowing the resin through the holes to the second side of the substrate, whereby the resin forms a single resin body encasing both of the integrated circuits (claim 17), before said encasing step, attaching a box to the second side of the substrate defining a volume for receiving the resin (claim 18), wherein the box includes openings defining exit paths for gas within the box (claim 19), wherein the encasing step comprises a molding operation performed at a pressure of less than one atmosphere (claim 20), wherein the substrate is laminar and at least the first face includes solder balls, the encasing step includes forming the resin on the first face such that the resin on the first face has a maximum distance from a plane of said substrate which is smaller than a maximum extension of the solder balls from the plane of the substrate (claim 21),wherein the solder balls are arranged in an array having a region without solder balls, and further comprising locating the first integrated circuit in said region (claim 22), wherein at least one of the first and second integrated circuits comprises a flip chip (claim 23), wherein the first integrated circuit comprises a flip chip (claim 24), wherein the flip chip is located in a recessed portion of the substrate (claim 25), and wherein the electrical contacts of at least one of the first and second integrated circuits are connected to electric contacts on the substrate by wire bonding (claim 26).

Thummel discloses wherein the substrate includes holes extending between the first face and the second face, the encasing step includes applying the resin to a first side of the substrate

and flowing the resin through the holes to the second side of the substrate, whereby the resin forms a single resin body encasing both of the integrated circuits (pg.1, paragraph 0008), before said encasing step, attaching a box to the second side of the substrate defining a volume for receiving the resin (Figure 1, reference 14), wherein the box includes openings defining exit paths for gas within the box (pg.3, paragraph 0042), wherein the encasing step comprises a molding operation performed at a pressure of less than one atmosphere (Figure 1, references 12 and 14), wherein the substrate is laminar and at least the first face includes solder balls, the encasing step includes forming the resin on the first face such that the resin on the first face has a maximum distance from a plane of said substrate which is smaller than a maximum extension of the solder balls from the plane of the substrate (pg.3, paragraphs 0045-0048; Figure 3), wherein the solder balls are arranged in an array having a region without solder balls, and further comprising locating the first integrated circuit in said region (pg.3, paragraph 0048), wherein at least one of the first and second integrated circuits comprises a flip chip (pg.3, paragraph 0048), wherein the first integrated circuit comprises a flip chip (pg.3, paragraph 0048; Figure 3), wherein the flip chip is located in a recessed portion of the substrate (Figure 12), and wherein the electrical contacts of at least one of the first and second integrated circuits are connected to electric contacts on the substrate by wire bonding (Figure 12, references 54A and 54B).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Seyyedy and Chhor et al, with the teachings of Thummel, for the purpose of encapsulating a substrate mounted electronic device.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seyyedy (6,780,675 B2) in view of Chhor et al (6,843,421 B2).

6. Regarding claim 29, Seyyedy discloses an integrated circuit package (Figure 3) comprising a substrate (Figure 4, reference 216) including electrical contacts (Figure 3, references 104 and 204) and integrated circuits attached to opposite sides of the substrate (Figure 3, references 102 and 202), the electrical contacts electrically connected to corresponding electrical contacts on the substrate (Figure 3). However, Seyyedy does not disclose each of the integrated circuits being encased in resin.

Chhor et al discloses encasing the first and second integrated circuits in resin (abstract).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Seyyedy with the teachings of Chhor et al, for the purpose of creating a memory module.

Claims 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seyyedy (6,780,675 B2) and Chhor et al (6,843,421 B2) in view of Thummel (US 2001/0045686 A1).

7. Seyyedy and Chhor et al discloses all above claimed subject matter except wherein a single resin body encases both the integrated circuits and extends through holes in the substrate (claim 30), wherein the electrical contacts of at least one of the integrated circuits are connected to the electrical contacts on the substrate by wire bonding (claim 31), solder balls are arranged on at least a first side of the substrate (claim 32), wherein the solder balls are arranged in an array having a region without solder balls, and wherein the first integrated circuit is located in said region (claim 33), wherein at least one of the integrated circuits comprises a flip chip (claim 34), and wherein the flip chip is located in a recessed portion of the substrate (claim 35).

Thummel discloses a single resin body encases both the integrated circuits and extends through holes in the substrate (pg.1, paragraphs 0008-0010), wherein the electrical contacts of at least one of the integrated circuits are connected to the electrical contacts on the substrate by wire bonding (Figure 12, references 54A and 54B), solder balls are arranged on at least a first side of the substrate (Figure 11, references 56A and 56B), wherein the solder balls are arranged in an array having a region without solder balls (pg.3, paragraph 0048), and wherein the first integrated circuit is located in said region (Figures 11 and 12), wherein at least one of the integrated circuits comprises a flip chip (pg.3, paragraph 0048; Figure 3), and wherein the flip chip is located in a recessed portion of the substrate (Figure 12).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Seyyedy and Chhor et al, with the teachings of Thummel, for the purpose of encapsulating a substrate mounted electronic device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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August 3, 2006

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